USB Charging Port Controller and Power Switch

Check for Samples: TPS2544

FEATURES

- **D+/D– CDP/DCP Modes per USB Battery Charging Specification 1.2**
- **D+/D– Shorted Mode per Chinese Telecommunication Industry Standard YD/T 1591-2009**
- **Support non-BC1.2 charging modes by automatic selection**
  - **D+/D– Divider Modes 2.0V/2.7V and 2.7/2.0V**
  - **D+/D- 1.2V Mode**
- **Supports Sleep-Mode Charging and Mouse/Keyboard Wake Up**
- **Automatic SDP/CDP Switching for devices that do not connect to CDP ports**
- **Compatible with USB 2.0 and 3.0 Power Switch requirements**
- **Integrated 73-mΩ (typ) High-Side MOSFET**
- **Adjustable Current-Limit up to 3.0 A (typ)**
- **Operating Range: 4.5V to 5.5V**
- **Max device current**
  - **2µA when device disabled**
  - **270µA when device enabled**
- **Drop-In and BOM Compatible with TPS2543 and TPS2546**
- **Available in 16-Pin QFN (3x3) Package**
- **8KV ESD rating on DM/DP pins**
- **UL Listed and CB File No. E169910**

APPLICATIONS

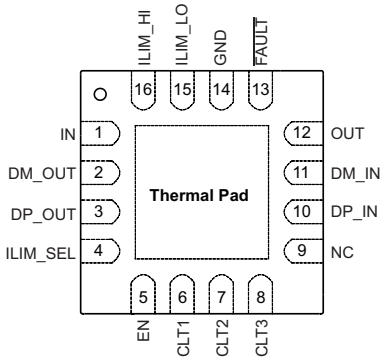
- **USB Ports (Host and Hubs)**
- **Notebook and Desktop PCs**
- **Universal Wall Charging Adapters**

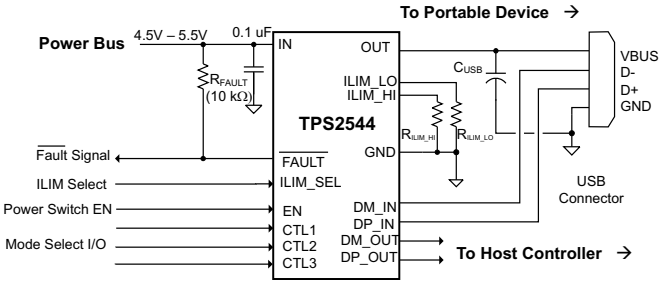
DESCRIPTION

The TPS2544 is a USB charging port controller and power switch with an integrated USB 2.0 high-speed data line (D+/D–) switch. TPS2544 provides the electrical signatures on D+/D– to support charging schemes listed under device feature section. TI tests charging of popular mobile phones, tablets and media devices with the TPS2544 to ensure compatibility with both BC1.2 compliant and non-compliant devices. In addition to charging popular devices, TPS2544 also supports system wake up (from S3) with a mouse/keyboard; both low speed and full speed are supported.

The TPS2544 73-mΩ power-distribution switch is intended for applications where heavy capacitive loads and short-circuits are likely to be encountered. Two programmable current thresholds provide flexibility for setting current limits.

TPS2544 RTE PACKAGE AND TYPICAL APPLICATION DIAGRAM





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE	DEVICE	TOP-SIDE MARKING
–40°C to 85°C	QFN16	TPS2544	2544

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range, voltages are referenced to GND (unless otherwise noted)

		LIMIT	UNIT
Voltage range	IN, EN, ILIM_LO, ILIM_HI, $\overline{\text{FAULT}}$, ILIM_SEL, CTL1, CTL2, CTL3, OUT	–0.3 to 7	V
	IN to OUT	–7 to 7	
	DP_IN, DM_IN, DP_OUT, DM_OUT	–0.3 to (IN + 0.3) or 5.7	
Input clamp current	DP_IN, DM_IN, DP_OUT, DM_OUT	±20	mA
Continuous current in SDP or CDP mode	DP_IN to DP_OUT or DM_IN to DM_OUT	±100	mA
Continuous current in BC1.2 DCP mode	DP_IN to DM_IN	±50	mA
Continuous output current	OUT	Internally limited	
Continuous output sink current	$\overline{\text{FAULT}}$	25	mA
Continuous output source current	ILIM_LO, ILIM_HI	Internally limited	mA
ESD rating	HBM	2	kV
	HBM wrt GND and each other, DP_IN, DM_IN, OUT	8	
	CDM	500	V
Operating junction temperature, T_J		–40 to Internally limited	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS2546 RTE (16 PIN)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	53.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	51.4	
θ_{JB}	Junction-to-board thermal resistance	17.2	
ψ_{JT}	Junction-to-top characterization parameter	3.7	
ψ_{JB}	Junction-to-board characterization parameter	20.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	3.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

voltages are referenced to GND (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage, IN	4.5		5.5	V
	Input voltage, logic-level inputs, EN, CTL1, CTL2, CTL3, ILIM_SEL	0		5.5	V
	Input voltage, data line inputs, DP_IN, DM_IN, DP_OUT, DM_OUT	0		V_{IN}	V
V_{IH}	High-level input voltage, EN, CTL1, CTL2, CTL3, ILIM_SEL	1.8			V
V_{IL}	Low-level input voltage, EN, CTL1, CTL2, CTL3, ILIM_SEL			0.8	V
	Continuous current, data line inputs, SDP or CDP mode, DP_IN to DP_OUT, DM_IN to DM_OUT			±30	mA
	Continuous current, data line inputs, BC1.2 DCP mode, DP_IN to DM_IN			±15	mA
I_{OUT}	Continuous output current, OUT	0		2.5	A
	Continuous output sink current, $\overline{FAULT}$	0		10	mA
R_{ILIM_XX}	Current-limit set resistors	16.9		750	kΩ
T_J	Operating virtual junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted: $–40 ≤ T_J ≤ 125°C$, $4.5V ≤ V_{IN} ≤ 5.5$ V, $V_{EN} = V_{IN}$, $V_{ILIM\_SEL} = V_{IN}$, $V_{CTL1} = V_{CTL2} = V_{CTL3} = V_{IN}$. $R_{\overline{FAULT}}$ = 10 kΩ, R_{ILIM_HI} = 20 kΩ, R_{ILIM_LO} = 80.6 kΩ. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH						
$R_{DS(on)}$	On resistance[1]	T_J = 25°C, I_{OUT} = 2 A		73	84	mΩ
		–40°C ≤ T_J ≤ 85°C, I_{OUT} = 2 A		73	105	
		–40°C ≤ T_J ≤ 125°C, I_{OUT} = 2 A		73	120	
t_r	OUT voltage rise time	V_{IN} = 5 V, C_L = 1 µF, R_L = 100 Ω (see Figure 20 and Figure 21)	0.7	1.0	1.60	ms
t_f	OUT voltage fall time		0.2	0.35	0.5	
t_{on}	OUT voltage turn-on time	V_{IN} = 5V, C_L = 1 µF, R_L = 100 Ω (see Figure 20 and Figure 22)		2.7	4	ms
t_{off}	OUT voltage turn-off time			1.7	3	
I_{REV}	Reverse leakage current	V_{OUT} = 5.5 V, $V_{IN} = V_{EN}$ = 0 V, –40 ≤ T_J ≤ 85°C, Measure I_{OUT}			2	µA
DISCHARGE						
R_{DCHG}	OUT discharge resistance	V_{OUT} = 4 V, V_{EN} = 0 V	400	500	630	Ω
t_{DCHG}	OUT discharge hold time	Time V_{OUT} < 0.7 V (see Figure 23)	1.30	2.0	2.9	s

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; Thermal effects must be taken into account separately.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted: –40 ≤ T_J ≤ 125°C, 4.5V ≤ V_{IN} ≤ 5.5 V, V_{EN} = V_{IN}, V_{ILIM_SEL} = V_{IN}, V_{CTL1} = V_{CTL2} = V_{CTL3} = V_{IN}. R $\overline{FAULT}$ = 10 kΩ, R_{ILIM_HI} = 20 kΩ, R_{ILIM_LO} = 80.6 kΩ. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN, ILIMSEL, CTL1, CTL2, CTL3 INPUTS						
	Input pin rising logic threshold voltage		1	1.35	1.70	V
	Input pin falling logic threshold voltage		0.85	1.15	1.45	
	Hysteresis (2)			200		mV
	Input current	Pin voltage = 0 V or 5.5 V	–0.5		0.5	µA
ILIMSEL CURRENT LIMIT						
I_{OS}	OUT short circuit current limit (3)	V_{ILIM_SEL} = 0 V, R_{ILIM_LO} = 210 kΩ	205	240	275	mA
		V_{ILIM_SEL} = 0 V, R_{ILIM_LO} = 80.6 kΩ	575	625	680	
		V_{ILIM_SEL} = 0 V, R_{ILIM_LO} = 22.1 kΩ	2120	2275	2430	
		V_{ILIM_SEL} = V_{IN}, R_{ILIM_HI}= 20 kΩ	2340	2510	2685	
		V_{ILIM_SEL} = V_{IN}, R_{ILIM_HI} = 16.9 kΩ	2770	2970	3170	
t_{IOS}	Response time to OUT short-circuit (2)	V_{IN} = 5.0 V, R = 0.1Ω, lead length = 2 inches (see Figure 24)		1.5		µs
SUPPLY CURRENT						
I_{IN_OFF}	Disabled IN supply current	V_{EN} = 0 V, V_{OUT} = 0 V, –40 ≤ T_J ≤ 85°C		0.1	2	µA
I_{IN_ON}	Enabled IN supply current	V_{CTL1} = V_{CTL2} = V_{IN}, V_{CTL3} = 0 V, V_{ILIM_SEL} = 0 V		165	220	µA
		V_{CTL1} = V_{CTL2} = V_{CTL3} = V_{IN}, V_{ILIM_SEL} = 0 V		175	230	
		V_{CTL1} = V_{CTL2} = V_{IN}, V_{CTL3} = 0V, V_{ILIM_SEL} = V_{IN}		185	240	
		V_{CTL1} = V_{CTL2} = V_{IN}, V_{CTL3} = VIN, V_{ILIM_SEL} = V_{IN}		195	250	
		V_{CTL1} = 0V, V_{CTL2} = V_{CTL3} = V_{IN}		215	270	
UNDERVOLTAGE LOCKOUT						
V_{UVLO}	IN rising UVLO threshold voltage		3.9	4.1	4.3	V
	Hysteresis (2)			100		mV
$\overline{FAULT}$						
	Output low voltage	$I_{\overline{FAULT}}$ = 1 mA			100	mV
	Off-state leakage	$V_{\overline{FAULT}}$ = 5.5 V			1	µA
	Over current $\overline{FAULT}$ rising and falling deglitch		5	8.2	12	ms
THERMAL SHUTDOWN						
	Thermal shutdown threshold		155			°C
	Thermal shutdown threshold in current-limit		135			
	Hysteresis (2)			20		

(2) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.
(3) Pulse-testing techniques maintain junction temperature close to ambient temperature; Thermal effects must be taken into account separately.

ELECTRICAL CHARACTERISTICS, HIGH-BANDWIDTH SWITCH

Unless otherwise noted: $-40 \le T_J \le 125°C$, $4.5\ V \le V_{IN} \le 5.5\ V$, $V_{EN} = V_{IN}$, $V_{ILIM\_SEL} = V_{IN}$, $V_{CTL1} = V_{CTL2} = V_{CTL3} = V_{IN}$. R $\overline{FAULT}$ = 10 kΩ, R_{ILIM_HI} = 20 kΩ, R_{ILIM_LO} = 80.6 kΩ, Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH-BANDWIDTH ANALOG SWITCH						
	DP/DM switch on resistance	V_{DP/DM_OUT} = 0 V, I_{DP/DM_IN} = 30 mA		2	4	Ω
		V_{DP/DM_OUT} = 2.4 V, I_{DP/DM_IN} = –15 mA		3	6	
	Switch resistance mismatch between DP / DM channels	V_{DP/DM_OUT} = 0 V, I_{DP/DM_IN} = 30 mA		0.05	0.15	Ω
		V_{DP/DM_OUT} = 2.4 V, I_{DP/DM_IN} = –15 mA		0.05	0.15	
	DP/DM switch off-state capacitance(1)	V_{EN} = 0 V, V_{DP/DM_IN} = 0.3 V, V_{ac} = 0.6 V_{pk-pk}, f = 1 MHz		3	3.6	pF
	DP/DM switch on-state capacitance(2)	V_{DP/DM_IN} = 0.3 V, V_{ac} = 0.6 V_{pk-pk}, f = 1 MHz		5.4	6.2	pF
O_{IRR}	Off-state isolation(3)	V_{EN} = 0 V, f = 250 MHz		33		dB
X_{TALK}	On-state cross channel isolation(3)	f = 250 MHz		52		dB
	Off state leakage current	V_{EN} = 0 V, V_{DP/DM_IN} = 3.6 V, V_{DP/DM_OUT} = 0 V, measure I_{DP/DM_OUT}		0.1	1.5	µA
BW	Bandwidth (–3dB)(3)	R_L = 50 Ω		2.6		GHz
t_{pd}	Propagation delay(3)			0.25		ns
t_{SK}	Skew between opposite transitions of the same port ($t_{PHL} – t_{PLH}$)			0.1	0.2	ns

(1) The resistance in series with the parasitic capacitance to GND is typically 250 Ω.
(2) The resistance in series with the parasitic capacitance to GND is typically 150 Ω
(3) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

ELECTRICAL CHARACTERISTICS, CHARGING CONTROLLER

Unless otherwise noted: –40 ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN} ≤ 5.5 V, V_{EN} = V_{IN}, V_{ILIM_SEL} = V_{IN}, V_{CTL1} = 0 V, V_{CTL2} = V_{CTL3} = V_{IN}. $R_{\overline{FAULT}}$ = 10 kΩ, R_{ILIM_HI} = 20 kΩ, R_{ILIM_LO} = 80.6 kΩ, Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SHORTED MODE (BC1.2 DCP)		**VCTL1 = VIN, VCTL2 = VCTL3 = 0V**				
	DP_IN / DM_IN shorting resistance			125	200	Ω
1.2V Mode						
	DP_IN /DM_IN output voltage		1.19	1.25	1.31	V
	DP_IN /DM_IN output impedance		60	75	94	kΩ
DIVIDER1 MODE						
	DP_IN Divider1 output voltage		1.9	2.0	2.1	V
	DM_IN Divider1 output voltage		2.57	2.7	2.84	V
	DP_IN output impedance		8	10.5	12.5	kΩ
	DM_IN output impedance		8	10.5	12.5	kΩ
DIVIDER2 MODE		**IOUT = 1A**				
	DP_IN Divider2 output voltage		2.57	2.7	2.84	V
	DM_IN Divider2 output voltage		1.9	2.0	2.1	V
	DP_IN output impedance		8	10.5	12.5	kΩ
	DM_IN output impedance		8	10.5	12.5	kΩ
CHARGING DOWNSTREAM PORT		**VCTL1 = VCTL2 = VCTL3 = VIN**				
V_{DM_SRC}	DM_IN CDP output voltage	V_{DP_IN} = 0.6 V, –250 µA < I_{DM_IN} < 0 µA	0.5	0.6	0.7	V
V_{DAT_REF}	DP_IN rising lower window threshold for V_{DM_SRC} activation		0.25		0.4	V
	Hysteresis (1)			50		mV
V_{LGC_SRC}	DP_IN rising upper window threshold for V_{DM_SRC} de-activation		0.8		1	V
	hysteresis (1)			100		mV
I_{DP_SINK}	DP_IN sink current	V_{DP_IN} = 0.6 V	40	70	100	µA

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TYPICAL CHARACTERISTICS

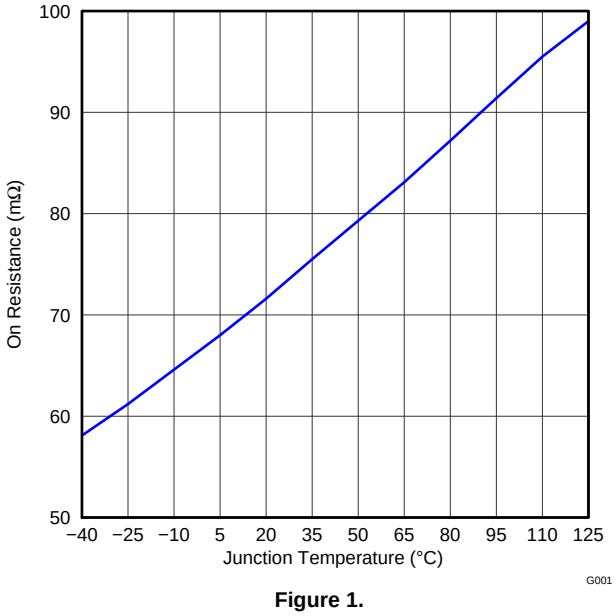


Figure 1.

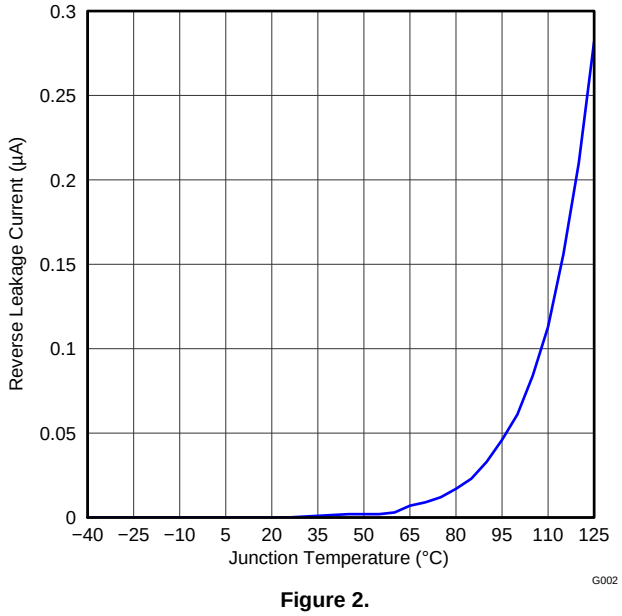


Figure 2.

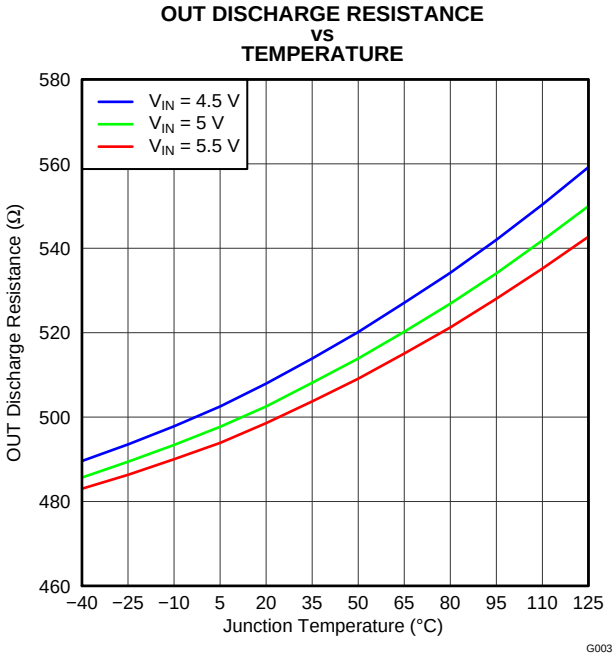


Figure 3.

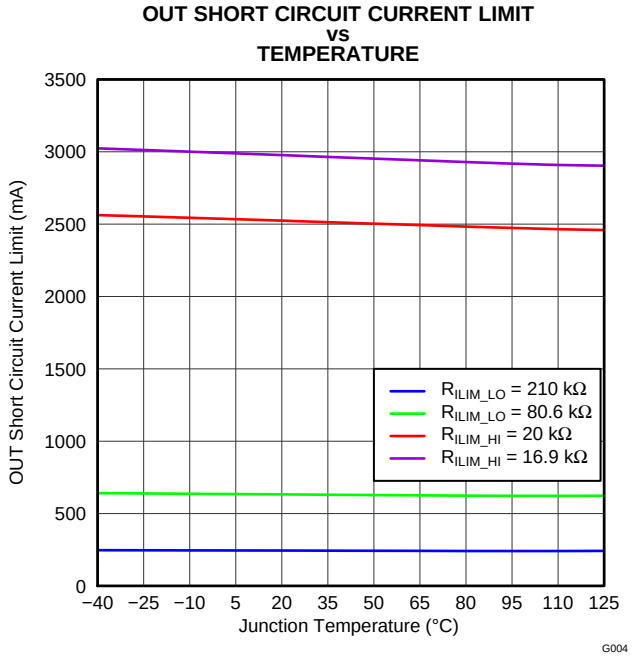


Figure 4.

TYPICAL CHARACTERISTICS (continued)

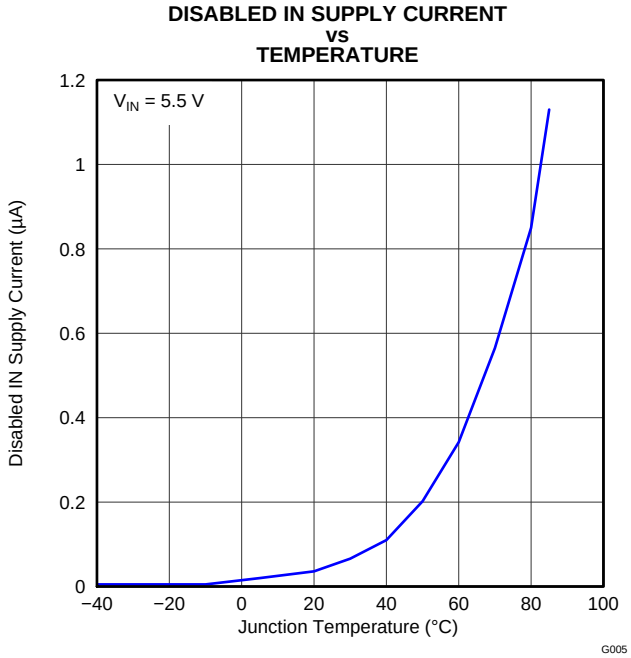


Figure 5.

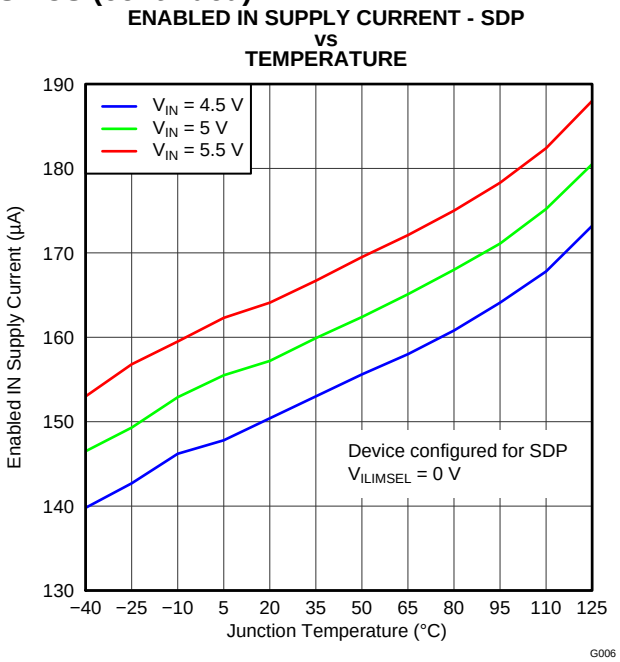


Figure 6.

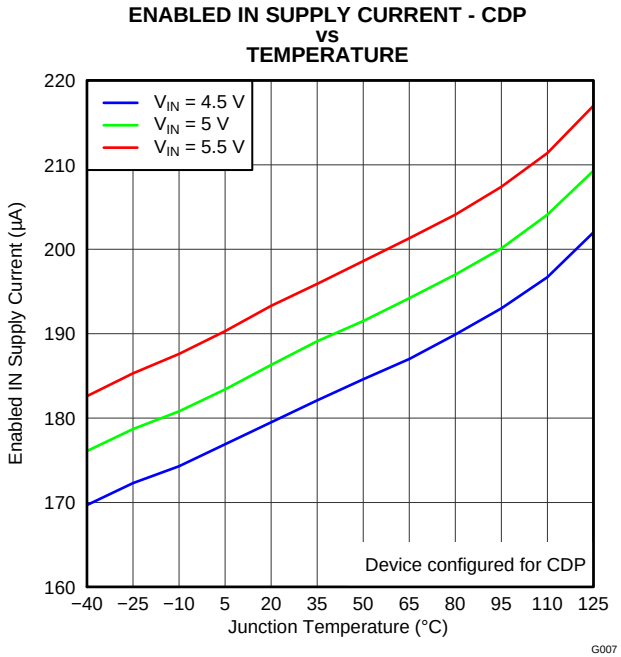


Figure 7.

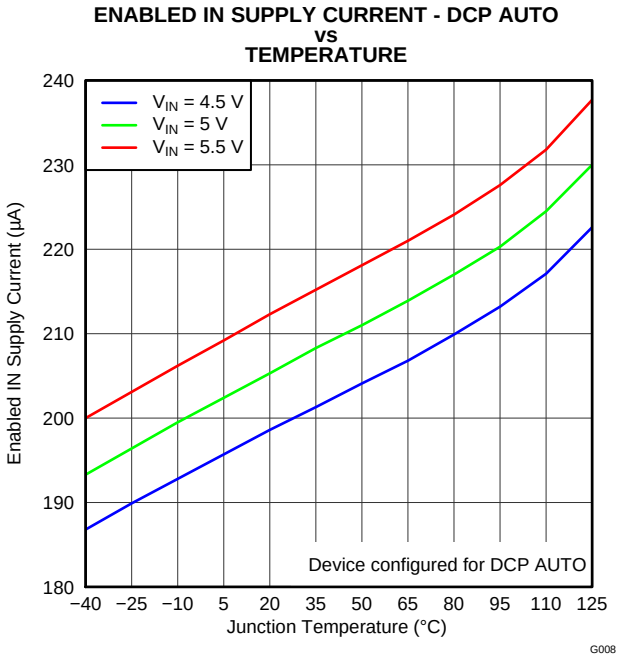


Figure 8.

TYPICAL CHARACTERISTICS (continued)

$\overline{\text{FAULT}}$ OUTPUT LOW VOLTAGE vs SINKING CURRENT

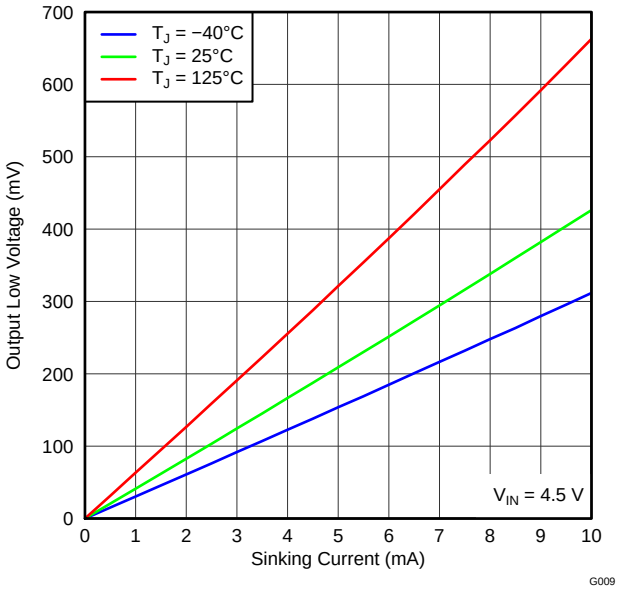


Figure 9.

DATA TRANSMISSION CHARACTERISTICS vs FREQUENCY

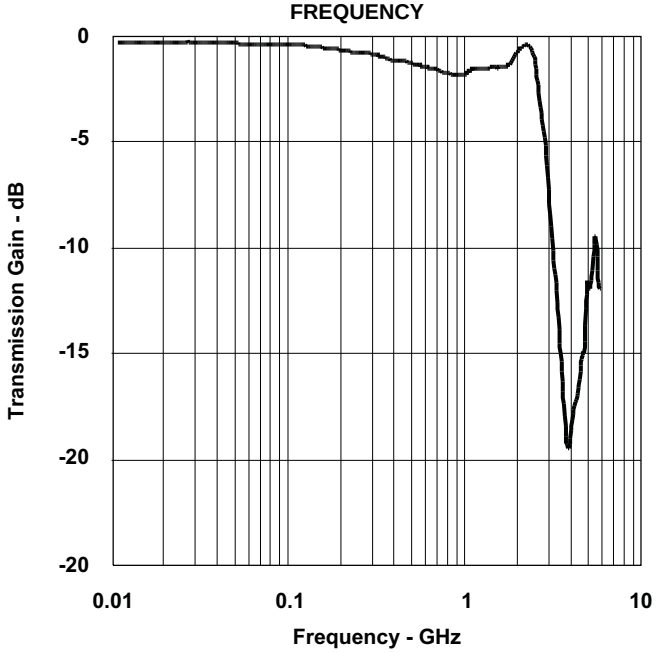


Figure 10.

OFF STATE DATA SWITCH ISOLATION vs FREQUENCY

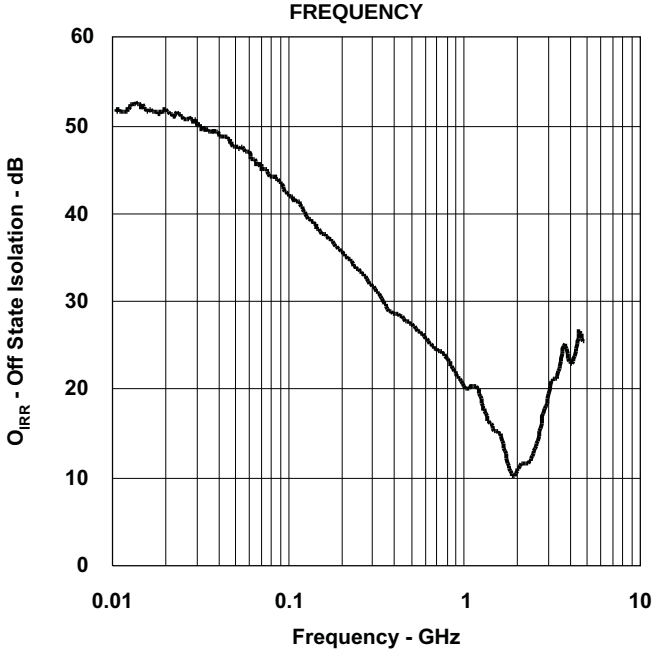


Figure 11.

ON STATE CROSS-CHANNEL ISOLATION vs FREQUENCY

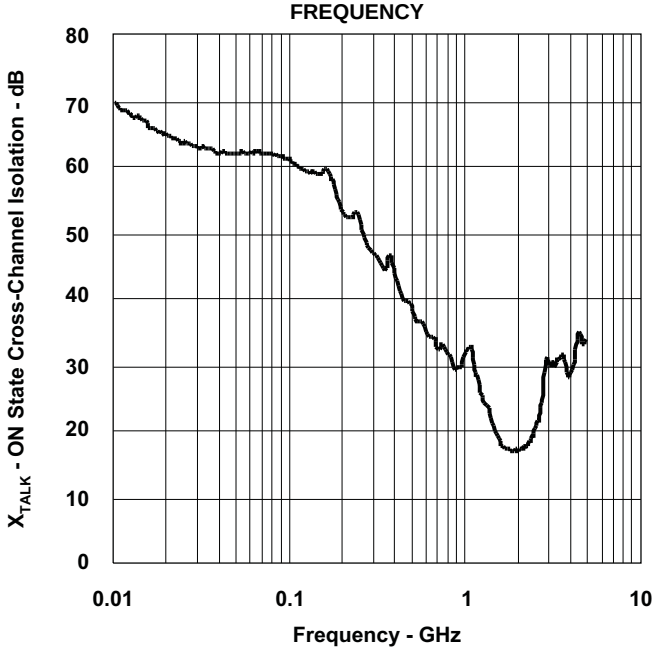


Figure 12.

TYPICAL CHARACTERISTICS (continued)

EYE DIAGRAM USING USB COMPLIANCE TEST PATTERN (with no switch)

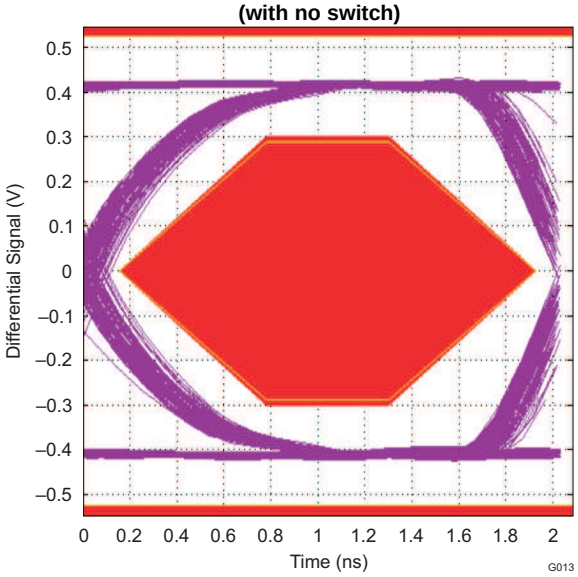


Figure 13.

EYE DIAGRAM USING USB COMPLIANCE TEST PATTERN (with data switch)

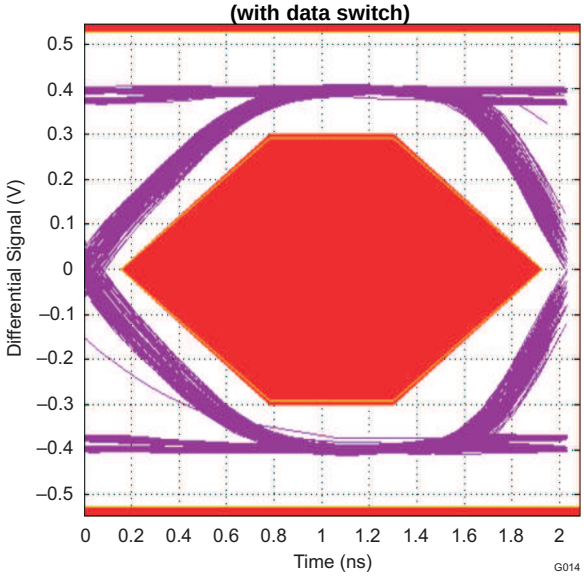


Figure 14.

TURN-ON RESPONSE

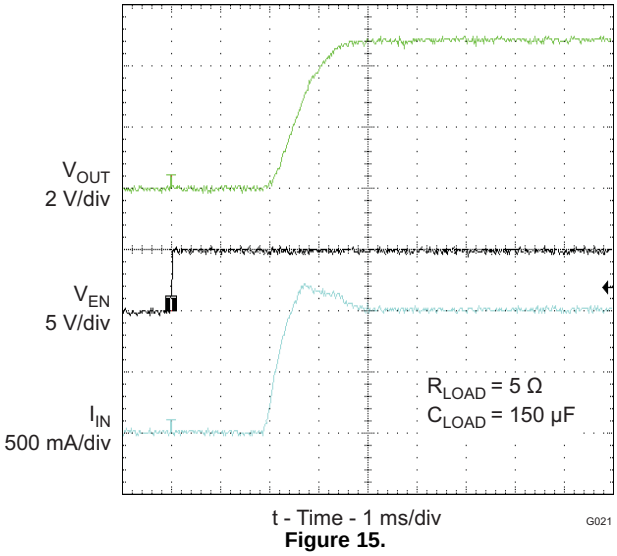


Figure 15.

TURN-OFF RESPONSE

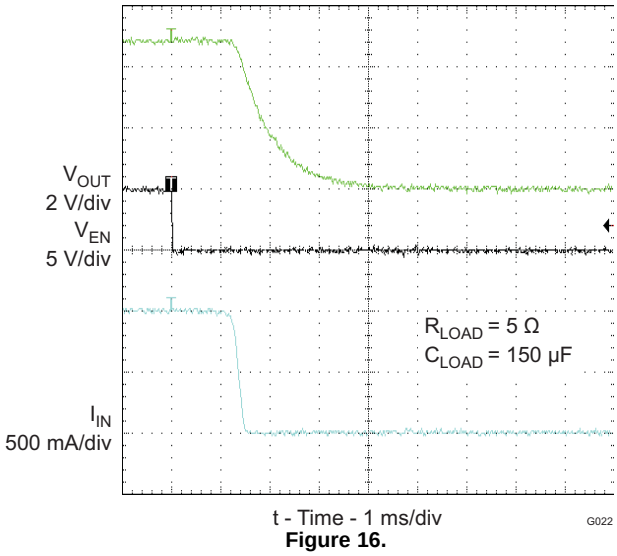


Figure 16.

TYPICAL CHARACTERISTICS (continued)

DEVICE ENABLED INTO SHORT CIRCUIT

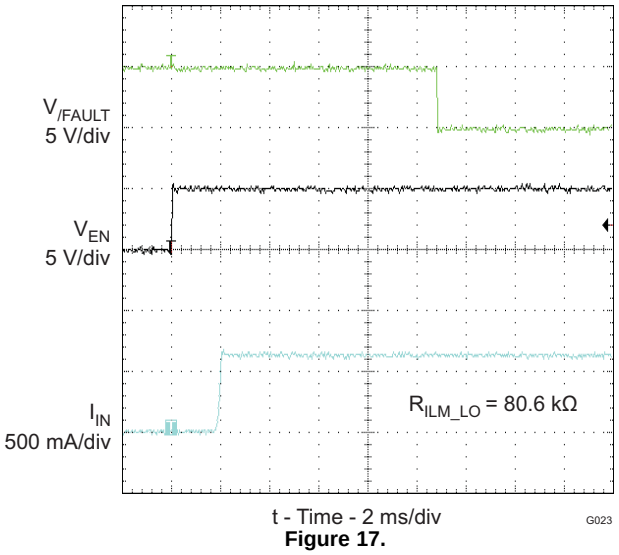


Figure 17.

DEVICE ENABLED INTO SHORT CIRCUIT - THERMAL CYCLING

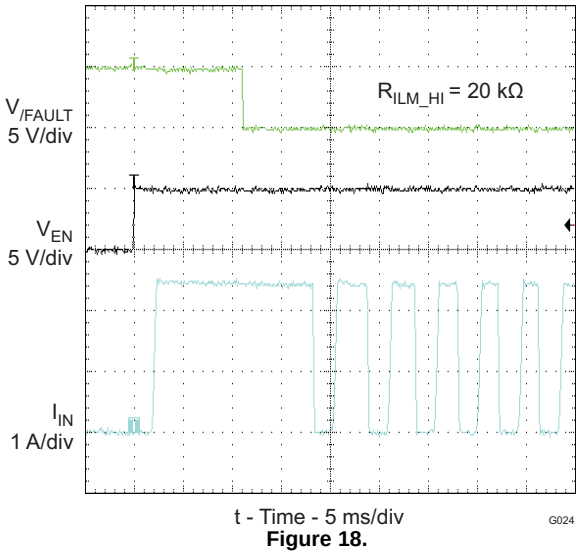


Figure 18.

SHORT CIRCUIT to FULL LOAD RECOVERY

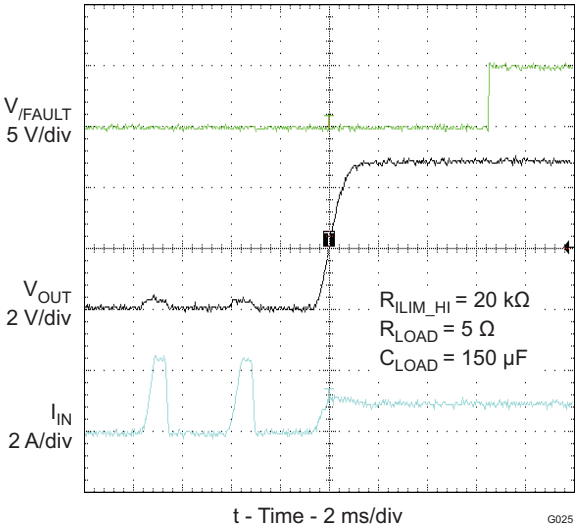


Figure 19.

PARAMETER MEASUREMENT DESCRIPTION

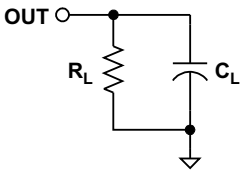


Figure 20. OUT Rise/Fall Test Load

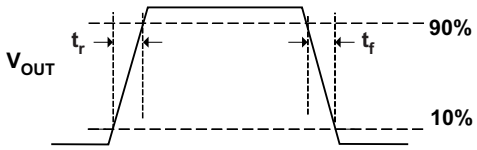


Figure 21. Power-On and Off Timing

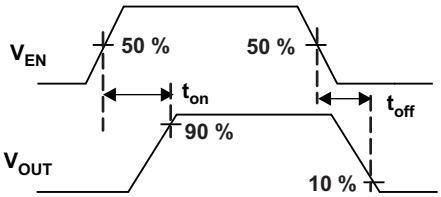


Figure 22. Enable Timing, Active High Enable

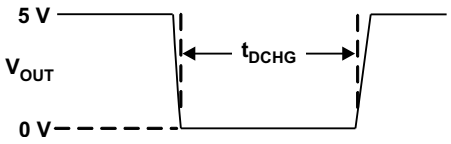


Figure 23. OUT Discharge During Mode Change

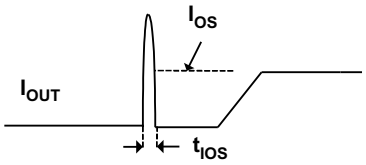
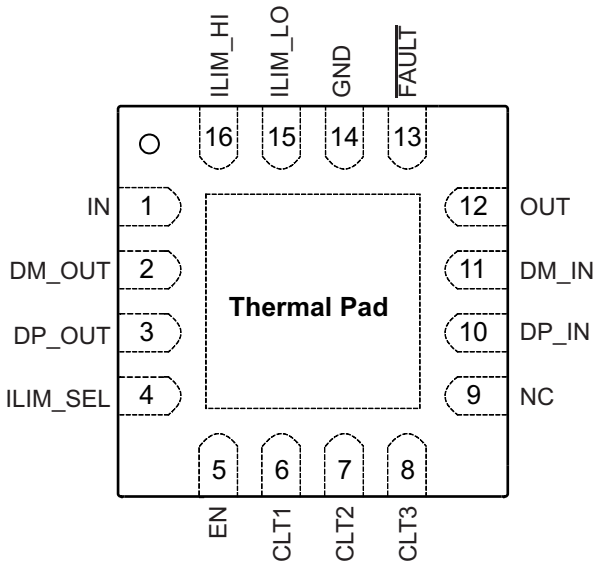


Figure 24. Output Short Circuit Parameters

DEVICE INFORMATION

TPS2544 RTE PACKAGE
(Top View)

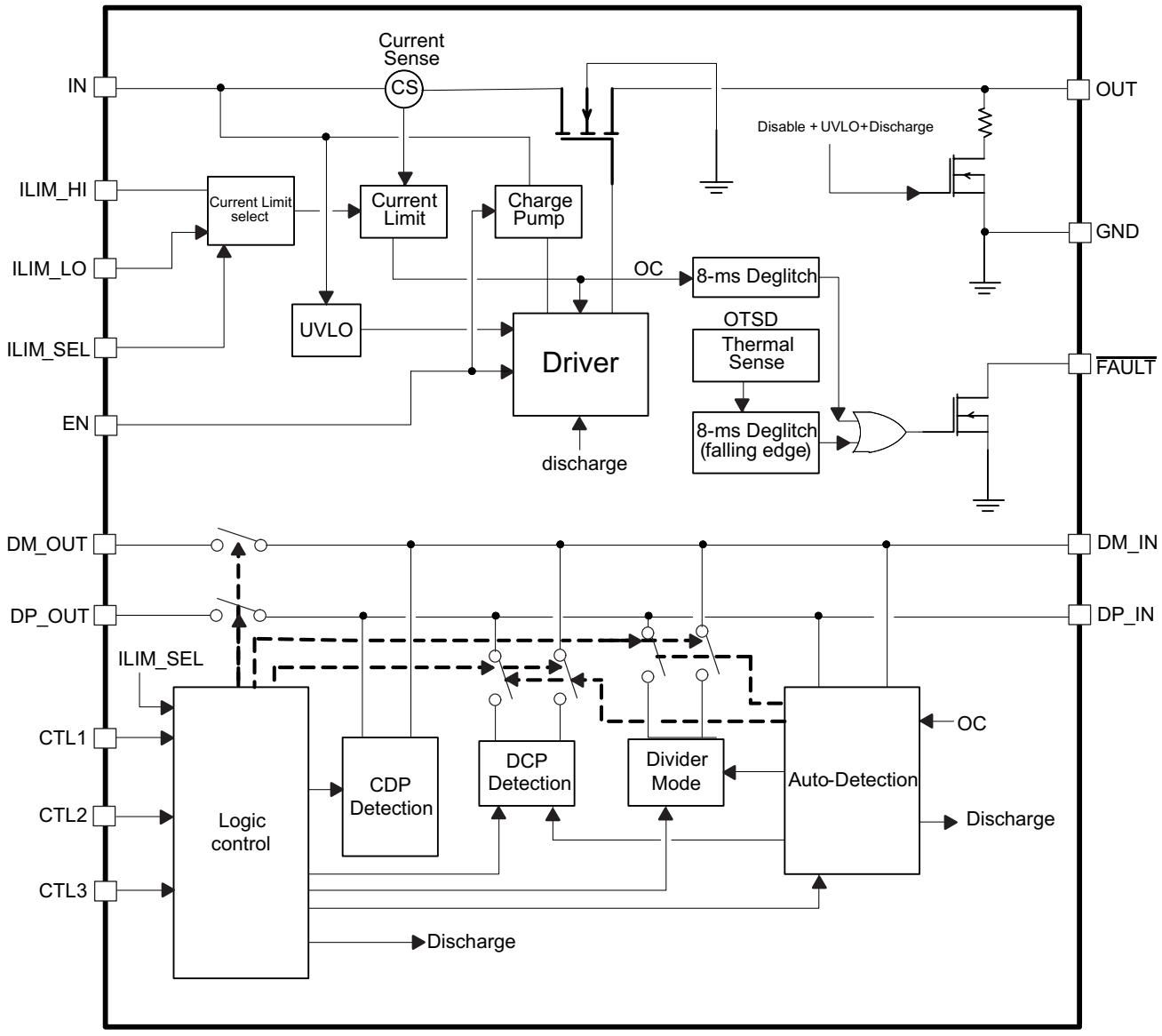


PIN FUNCTIONS

NO.	NAME	TYPE(1)	DESCRIPTION
1	IN	P	Input voltage and supply voltage; connect 0.1 µF or greater ceramic capacitor from IN to GND as close to the device as possible
2	DM_OUT	I/O	D– data line to USB host controller
3	DP_OUT	I/O	D+ data line to USB host controller
4	ILIM_SEL	I	Logic-level input signal used to control the charging mode current limit threshold; see the control truth table. Can be tied directly to IN or GND without pull-up or pull-down resistor.
5	EN	I	Logic-level input for turning the power switch and the signal switches on/off; logic low turns off the signal and power switches and holds OUT in discharge. Can be tied directly to IN or GND without pull-up or pull-down resistor.
6	CTL1	I	Logic-level inputs used to control the charging mode and the signal switches; see the control truth table. Can be tied directly to IN or GND without pull-up or pull-down resistor.
7	CTL2	I	
8	CTL3	I	
9	-	N/C	Connect to GND or leave open
10	DP_IN	I/O	D+ data line to downstream connector
11	DM_IN	I/O	D– data line to downstream connector
12	OUT	P	Power-switch output
13	$\overline{\text{FAULT}}$	O	Active-low open-drain output, asserted during over-temperature or current limit conditions
14	GND	P	Ground connection
15	ILIM_LO	I	External resistor connection used to set the low current-limit threshold. A resistor to ILIM_LO is optional; see Current-Limit Settings in DETAILED DESCRIPTION.
16	ILIM_HI	I	External resistor connection used to set the high current-limit threshold
NA	PowerPAD		Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect to GND plane.

(1) G = Ground, I = Input, O = Output, P = Power, N/C = No Connect

TPS2544 FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

Overview

The following overview references various industry standards. It is always recommended to consult the most up-to-date standard to ensure the most recent and accurate information. Rechargeable portable equipment requires an external power source to charge its batteries. USB ports are a convenient location for charging because of an available 5V power source. Universally accepted standards are required to make sure host and client-side devices operate together in a system to ensure power management requirements are met. Traditionally, host ports following the USB 2.0 specification must provide at least 500mA to downstream client-side devices. Because multiple USB devices can be attached to a single USB port through a bus-powered hub, it is the responsibility of the client-side device to negotiate its power allotment from the host to ensure the total current draw does not exceed 500mA. In general, each USB device is granted 100mA and may request more current in 100mA unit steps up to 500mA. The host may grant or deny based on the available current. A USB 3.0 host port not only provides higher data rate than USB 2.0 port but also raises the unit load from 100mA to 150mA. It is also required to provide a minimum current of 900mA to downstream client-side devices.

Additionally, the success of USB has made the mini-USB connector a popular choice for wall adapter cables. This allows a portable device to charge from both a wall adapter and USB port with only one connector. As USB charging has gained popularity, the 500mA minimum defined by USB 2.0 or 900mA for USB 3.0 has become insufficient for many handset and personal media players which need a higher charging rate. Wall adapters can provide much more current than 500mA/900mA. Several new standards have been introduced defining protocol handshaking methods that allow host and client devices to acknowledge and draw additional current beyond the 500mA/900mA minimum defined by USB 2.0/3.0 while still using a single micro-USB input connector.

The TPS2544 supports four of the most common USB charging schemes found in popular hand-held media and cellular devices:

- USB Battery Charging Specification BC1.2
- Chinese Telecommunications Industry Standard YD/T 1591-2009
- Divider Mode
- 1.2V Mode

YD/T 1591-2009 is a subset of BC1.2 spec. supported by vast majority of devices that implement USB changing. Divider and 1.2V charging schemes are supported in devices from specific yet popular device makers.

BC1.2 lists three different port types as listed below.

- Standard Downstream Port (SDP)
- Charging Downstream Port (CDP)
- Dedicated Charging Port (DCP)

BC1.2 defines a charging port as a downstream facing USB port that provides power for charging portable equipment, under this definition CDP and DCP are defined as charging ports

Table 1 shows the differences between these ports.

Table 1. Operating Modes

PORT TYPE	SUPPORT USB 2.0 COMMUNICATION	MAX. ALLOWABLE CURRENT DRAW BY PORTABLE DEVICE (A)
SDP (USB 2.0)	Yes	0.5
SDP (USB 3.0)	Yes	0.9
CDP	Yes	1.5
DCP	No	1.5

Standard Downstream Port (SDP) USB 2.0/USB 3.0

An SDP is a traditional USB port that follows USB 2.0/3.0 protocol and supplies a minimum of 500mA/900mA per port. USB 2.0/3.0 communications is supported, and the host controller must be active to allow charging. TPS2544 supports SDP mode in system power state S0 when system is completely powered ON and fully operational. For more details on control pin (CTL1-CTL3) settings to program this state please refer to device truth table.

Charging Downstream Port (CDP)

A CDP is a USB port that follows USB BC1.2 and supplies a minimum of 1.5A per port. It provides power and meets USB 2.0 requirements for device enumeration. USB 2.0 communications is supported, and the host controller must be active to allow charging. What separates a CDP from an SDP is the host-charge handshaking logic that identifies this port as a CDP. A CDP is identifiable by a compliant BC1.2 client device and allows for additional current draw by the client device.

The CDP hand-shaking process is done in two steps. During step one the portable equipment outputs a nominal 0.6V output on its D+ line and reads the voltage input on its D- line. The portable device concludes it is connected to an SDP if the voltage is less than the nominal data detect voltage of 0.3V. The portable device concludes that it is connected to a Charging Port if the D- voltage is greater than the nominal data detect voltage of 0.3V and optionally less than 0.8V.

The second step is necessary for portable equipment to determine if it is connected to CDP or DCP. The portable device outputs a nominal 0.6V output on its D- line and reads the voltage input on its D+ line. The portable device concludes it is connected to a CDP if the data line being read remains less than the nominal data detect voltage of 0.3V. The portable device concludes it is connected to a DCP if the data line being read is greater than the nominal data detect voltage of 0.3V.

TPS2544 supports CDP mode in system power state S0 when system is completely powered ON and fully operational. For more details on control pin (CTL1-CTL3) settings to program this state please refer to device truth table.

Dedicated Charging Port (DCP)

A DCP only provides power but does not support data connection to an upstream port. As shown in following sections, a DCP is identified by the electrical characteristics of its data lines. The TPS2544 emulates DCP in two charging states, namely DCP Forced and DCP Auto as shown in Figure 32. In DCP Forced state the device will support one of the two DCP charging schemes, namely Divider1 or Shorted. In the DCP Auto state, the device charge detection state machine is activated to selectively implement charging schemes involved with the Shorted, Divider1, Divider2, and 1.2V modes. Shorted DCP mode complies with BC1.2 and Chinese Telecommunications Industry Standard YD/T 1591-2009, while the Divider and 1.2V modes are employed to charge devices that do not comply with BC1.2 DCP standard.

DCP BC1.2 and YD/T 1591-2009

Both standards define that the D+ and D- data lines should be shorted together with a maximum series impedance of 200 Ω. This is shown in Figure 25.

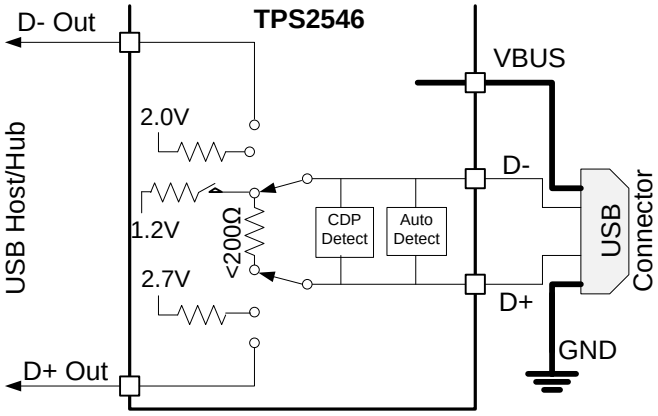


Figure 25. DCP Supporting BC1.2/YD/T 1591-2009

DCP Divider Charging Scheme

There are two Divider charging scheme supported by the device, Divider1 and Divider2 as shown in Figure 26 and Figure 27. In Divider1 charging scheme the device applies 2.0V and 2.7V to D+ and D- data line respectively. This is reversed in Divider2 mode.

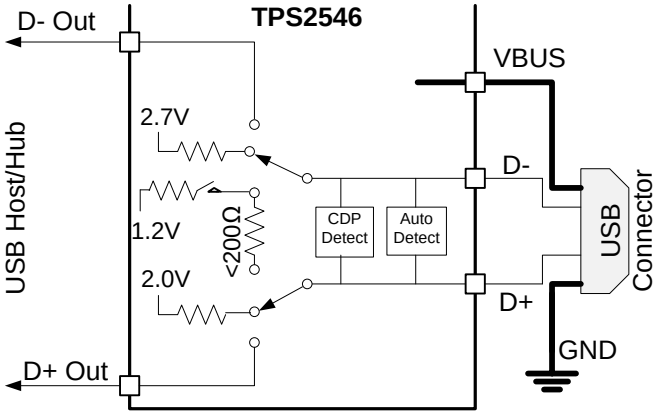


Figure 26. DCP Divider1 Charging Scheme

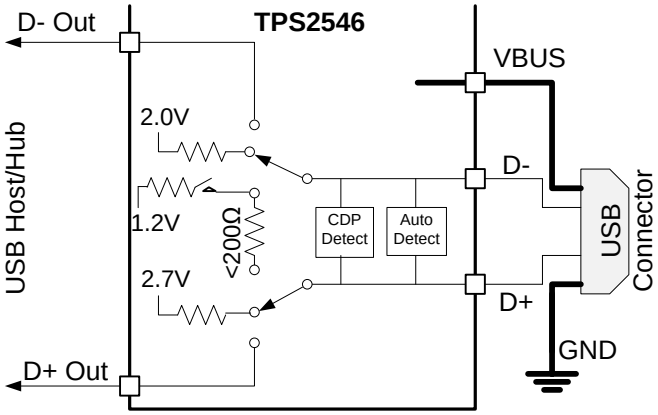


Figure 27. Divider2 Charging Scheme

DCP 1.2V Charging Scheme

1.2V charging scheme is used by some handheld devices to enable fast charging at 2.0A. TPS2544 supports this scheme in the DCP-Auto mode before the device enters BC1.2 shorted mode. To simulate this charging scheme D+/D- lines are shorted and pulled-up to 1.2V for fixed duration then device moves to DCP shorted mode as defined in BC1.2 spec. This is shown in Figure 28

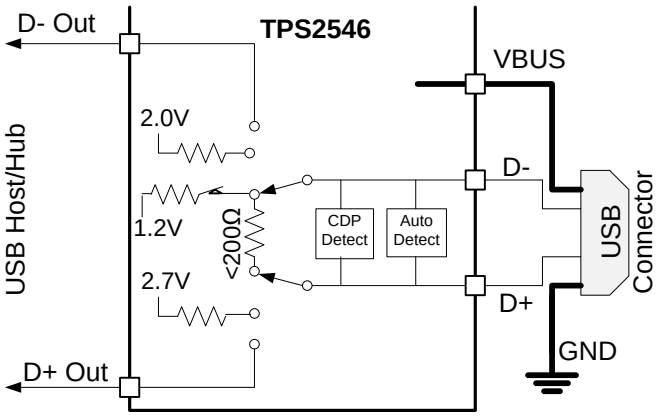


Figure 28. DCP 1.2V Charging Scheme

DCP Auto Mode

As mentioned above the TPS2544 integrates an auto-detect state machine that supports all the above DCP charging schemes. It starts in Divider1 scheme, however if a BC1.2 or YD/T 1591-2009 compliant device is attached, the TPS2544 responds by discharging OUT, turning back on the power switch and operating in 1.2V mode briefly and then moving to BC1.2 DCP mode. It then stays in that mode until the device releases the data line, in which case it goes back to Divider1 scheme. When a Divider1 compliant device is attached the TPS2544 will stay in Divider1 state.

Also, the TPS2544 will automatically switch between the Divider1 and Divider2 schemes based on charging current drawn by the connected device. Initially the device will set the data lines to Divider1 scheme. If charging current of >750mA is measured by the TPS2544 it switches to Divider2 scheme and test to see if the peripheral device will still charge at a high current. If it does then it stays in Divider2 scheme otherwise it will revert to Divider1 scheme

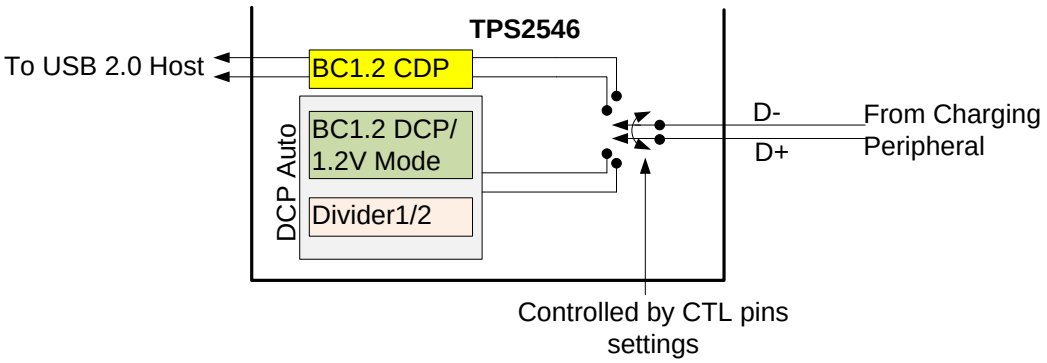


Figure 29. DCP Auto Mode

DCP Forced Shorted / DCP Forced Divider1

In this mode the device is permanently set to one of the DCP schemes (BC1.2/ YD/T 1591-2009 or Divider1) as commanded by its control pin setting per device truth table.

High-Bandwidth Data Line Switch

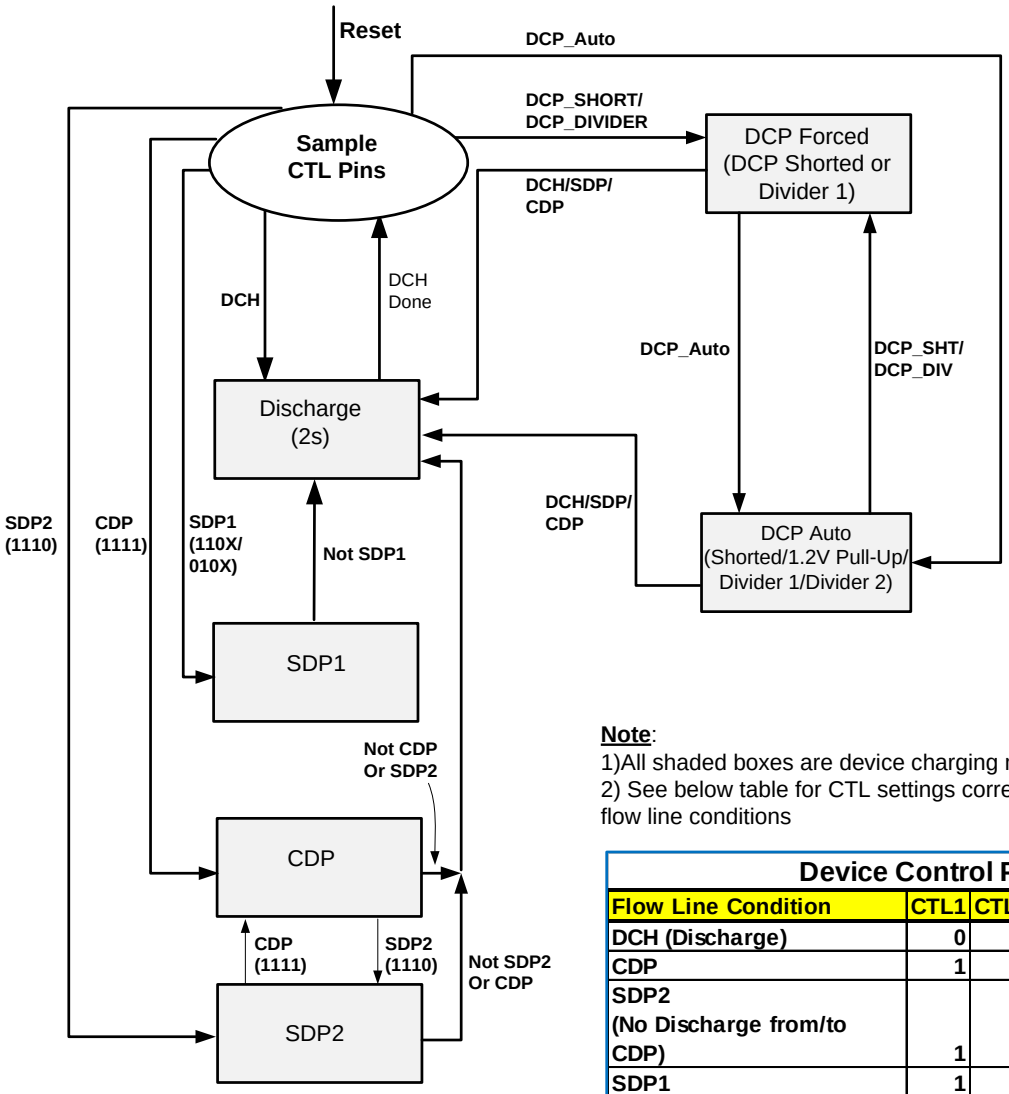
The TPS2544 passes the D+ and D- data lines through the device to enable monitoring and handshaking while supporting charging operation. A wide bandwidth signal switch is used, allowing data to pass through the device without corrupting signal integrity. The data line switches are turned on in any of CDP or SDP operating modes. The EN input also needs to be at logic High for the data line switches to be enabled.

NOTE

1. While in CDP mode, the data switches are ON even while CDP handshaking is occurring.
2. The data line switches are OFF if EN or all CTL pins are held low, or if in DCP mode. They are not automatically turned off if the power switch (IN to OUT) is in current limit.
3. The data switches are for USB 2.0 differential pair only. In the case of a USB 3.0 host, the super speed differential pairs must be routed directly to the USB connector without passing through the TPS2544.
4. Data switches are OFF during OUT (VBUS) discharge

Device Operation

Please refer to the simplified device state diagram in Figure 30. Power-on-reset (POR) holds device in initial state while output is held in discharge mode. Any POR event will take the device back to initial state. After POR clears, device goes to the next state depending on the CTL lines as shown in Figure 30.



Note:
1)All shaded boxes are device charging modes
2) See below table for CTL settings corresponding to flow line conditions

Device Control Pins				
Flow Line Condition	**CTL1**	**CTL2**	**CTL3**	**ILIM_SEL**
DCH (Discharge)	0	0	0	X
CDP	1	1	1	1
SDP2 (No Discharge from/to CDP)	1	1	1	0
SDP1	1	1	0	X
(Discharge from/to any charging state including CDP)	0	1	0	X
DCP_SHORT	1	0	0	X
DCP_DIVIDER	1	0	1	X
DCP_Auto	0	1	1	X
	0	0	1	X

Figure 30. TPS2544 Charging States

Output Discharge

To allow a charging port to renegotiate current with a portable device, TPS2544 uses the OUT discharge function. It proceeds by turning off the power switch while discharging OUT, then turning back on the power switch to reassert the OUT voltage. This discharge function is automatically applied as shown in device state diagram.

Wake on USB Feature (Mouse/Keyboard Wake Feature)

USB 2.0 Background Information

The TPS2544 data lines interface with USB 2.0 devices. USB 2.0 defines three types of devices according to data rate. These devices and their characteristics relevant to TPS2544 Wake on USB operation are shown below

Low-speed USB devices

- 1.5 Mb/s
- Wired mice and keyboards are examples
- No devices that need battery charging
- All signaling performed at 2.0V and 0.8V hi/lo logic levels
- D- high to signal connect and when placed into suspend
- D- high when not transmitting data packets

Full-speed USB devices

- 12 Mb/s
- Wireless mice and keyboards are examples
- Legacy phones and music players are examples
- Some legacy devices that need battery charging
- All signaling performed at 2.0V and 0.8V hi/lo logic levels
- D+ high to signal connect and when placed into suspend
- D+ high when not transmitting data packets

High-speed USB devices

- 480 Mb/s
- Tablets, phones and music players are examples
- Many devices that need battery charging
- Connect and suspend signaling performed at 2.0V and 0.8V hi/lo logic levels
- Data packet signaling performed a logic levels below 0.8V
- D+ high to signal connect and when placed into suspend (same as a full-speed device)
- D+ and D- low when not transmitting data packets

Wake On USB

Wake on USB is the ability of a wake configured USB device to wake a computer system from its S3 sleep state back to its S0 working state. Wake on USB requires the data lines to be connected to the system USB host before the system is placed into its S3 sleep state and remain continuously connected until they are used to wake the system.

The TPS2544 supports low and high speed HID (human interface device like mouse/key board) wake function. There are two scenarios under which wake on mouse are supported by the TPS2544. The specific CTL pin changes that the TPS2544 will override are shown below. The information is presented as CTL1, CTL2, CTL3. The ILIM_SEL pin plays no role

1. 111 (CDP/SDP2) to 011 (DCP-Auto)
2. 010 (SDP1) to 011 (DCP-Auto)

Note that the 110 (SDP1) to 011 (DCP-Auto) transition is not supported. This is done for practical reasons since the transition involves changes to two CTL pins. Depending on which CTL pin changes first, the device will see either a temporary 111 or 010 command. The 010 command is safe but the 111 command will cause an OUT discharge as the TPS2544 will instead proceed to the 111 state.

USB Slow-Speed / Full-Speed Device Recognition

TPS2544 is capable of detecting LS or FS device attachment when TPS2544 is in SDP or CDP mode. Per USB spec when no device is attached, the D+ and D- lines are near ground level. When a low speed compliant device is attached to the TPS2544 charging port, D- line will be pulled high in its idle state (mouse/keyboard not activated). However when a FS device is attached the opposite is true in its idle state, i.e. D+ is pulled high and D- remains at ground level.

TPS2544 monitors both D+ and D- lines while CTL pin settings are in CDP or SDP mode to detect LS or FS HID device attachment. To support HID sleep wake, TPS2544 must first determine that it is attached to a LS or FS device when system is in S0 power state. TPS2544 does this as described above. While supporting a LS HID wake is straight forward, supporting FS HID requires making a distinction between a FS and a HS device. This is because a high speed device will always present itself initially as a full speed device (by a 1.5K pull up resistor on D+). The negotiation for high speed then makes the distinction whereby the 1.5K pull up resistor gets removed.

TPS2544 handles the distinction between a FS and HS device at connect by memorizing if the D+ line goes low after connect. A HS device after connect will always undergo negotiation for HS which will require the 1.5KΩ resistor pull-up on D+ to be removed. To memorize a FS device, TPS2544 requires the device to remain connected for at least 60 sec while system is in S0 mode before placing it in sleep or S3 mode. *If system is placed in sleep mode earlier than the 60 sec window, a FS device may not get recognized and hence could fail to wake system from S3.*This requirement does not apply for LS device.

No CTL Pin Timing Requirement After Wake Event and Transition from S3 to S0

Unlike the TPS2543, there is no CTL pin timing requirement for the TPS2544 when the wake configured USB device wakes the system from S3 back to S0. The TPS2543 requires the CTL pins to transition from the DCP-Auto setting back to the SDP/CDP setting within 64ms of the attached USB device signaling a wake event (e.g. mouse clicked or keyboard key pressed). No such timing condition exists for the TPS2544.

Device Truth Table (TT)

Device TT lists all valid bias combinations for the three control pins CTL1-3 and ILIM_SEL pin and their corresponding charging mode. It is important to note that the TT *purposely* omits matching charging modes of the TPS2544 with global power states (S0-S5) as device is agnostic to system power states. The TPS2544 monitors its CTL inputs and will transition to whatever charging state it is commanded to go to (except when LS/FS HID device is detected). For example if sleep charging is desired when system is in standby or hibernate state then user must set TPS2544 CTL pins to correspond to DCP_Auto charging mode per below table. When system is put back to operation mode then set control pins to correspond to SDP or CDP mode and so on.

Table 2. Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	MODE	CURRENT LIMIT SETTING	COMMENT
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	
0	X	1	X	DCP_Auto	ILIM_HI	Data Lines Disconnected
0	1	0	0	SDP1	ILIM_LO	Data Lines connected
0	1	0	1	SDP1	ILIM_HI	
0	1	1	0	DCP_Auto	ILIM_HI	Data Lines Disconnected
0	1	1	1	DCP_Auto	ILIM_HI	Data Lines Disconnected
1	0	0	0	DCP _Shorted	ILIM_LO	Device Forced to stay in DCP BC1.2 charging mode
1	0	0	1	DCP_Shorted	ILIM_HI	
1	0	1	0	DCP / Divider1	ILIM_LO	Device Forced to stay in DCP Divider1 Charging Mode
1	0	1	1	DCP / Divider1	ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	Data Lines Connected
1	1	0	1	SDP1	ILIM_HI	
1	1	1	0	SDP2(1)	ILIM_LO	
1	1	1	1	CDP(1)	ILIM_HI	Data Lines Connected

(1) No OUT discharge when changing between 1111 and 1110.

Table 3 can be used as an *aid* to program the TPS2544 per system states however not restricted to below settings only.

Table 3. Control Pin Settings Matched to System Power States

SYSTEM GLOBAL POWER STATE	TPS2544 CHARGING MODE	CTL1	CTL2	CTL3	ILIM_SEL	CURRENT LIMIT SETTING
S0	SDP1	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP2, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP	1	1	1	1	ILIM_HI
S3/S4/S5	Auto mode	0	0	1	0	ILIM_HI
S3	Auto mode, keyboard/mouse wake-up	0	1	1	0	ILIM_HI
S3	SDP1, keyboard/mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO

CDP/SDP Auto Switch

TPS2544 is equipped with a CDP/SDP auto-switch feature to support some popular phones in the market that are not compliant to the BC1.2 specification, as they fail to establish data connection in CDP mode. These phones use primary detection (used to distinguish between an SDP and different types of Charging Ports) to only identify ports as SDP (data / no charge) or DCP (no data / charge). They do not recognize CDP (data /charge) ports. When connected to a CDP port, these phones classify the port as a DCP and will only charge. Since charging ports are configured as CDP when the computer is in S0, users do not get the expected data connection. See Figure 39

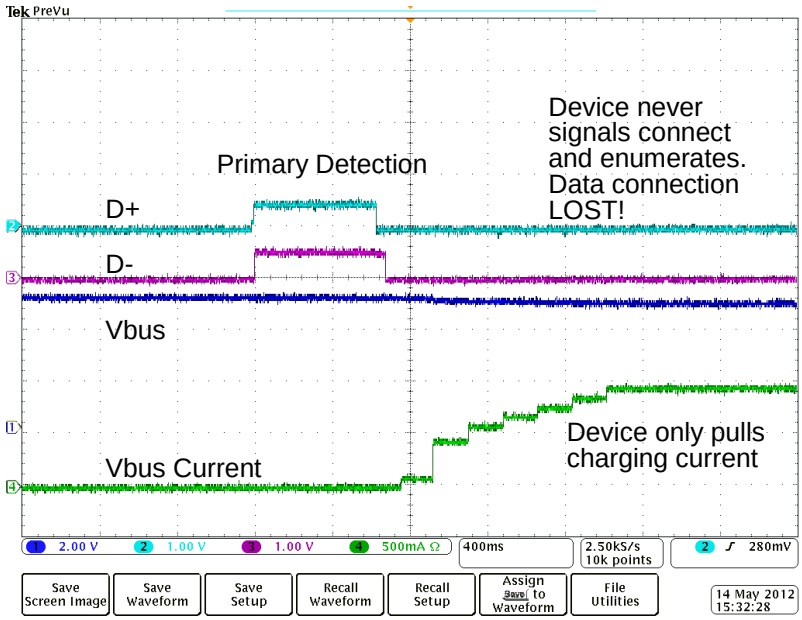


Figure 31. CDP/SDP Auto

To remedy this problem TPS2544 employs a CDP/SDP Auto Switch scheme to ensure these BC1.2 non-compliant phones will establish data connection by following below steps:

- The TPS2544 will determine when a non-compliant phone has wrongly classified a CDP port as a DCP port and has not made a data connection
- The TPS2544 will then automatically do a OUT (VBUS) discharge and reconfigure the port as an SDP
- This allows the phone to discover it is now connected to an SDP and establish a data connection
- The TPS2544 will then switch automatically back to CDP without doing an OUT (VBUS) discharge
- The phone will continue to operate like it is connected to a SDP since OUT (VBUS) was not interrupted
- The port is now ready in CDP if a new device is attached

Over-Current Protection

When an over-current condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before VIN has been applied. The TPS2544 senses the short and immediately switches into a constant-current output. In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for nominally one to two microseconds before the current-limit circuit can react. The device operates in constant-current mode after the current-limit circuit has responded. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting. The device will remain off until the junction temperature cools approximately 20°C and will then re-start. The device will continue to cycle on/off until the over-current condition is removed.

Current-Limit Settings

The TPS2544 has two independent current limit settings that are each programmed externally with a resistor. The ILIM_HI setting is programmed with R_{ILIM_HI} connected between ILIM_HI and GND. The ILIM_LO setting is programmed with R_{ILIM_LO} connected between ILIM_LO and GND. Consult the Device Truth Table (Table 2) to see when each current limit is used. Both settings have the same relation between the current limit and the programming resistor.

R_{ILIM_LO} is optional and the ILIM_LO pin may be left unconnected if the following condition is met:

- ILIM_SEL is always set high

The following equation programs the typical current limit:

$$I_{OS\_typ}(mA) = \frac{50,250}{R_{ILIM\_XX}(k\Omega)} \quad (1)$$

R_{ILIM_XX} corresponds to either R_{ILIM_HI} or R_{ILIM_LO} as appropriate.

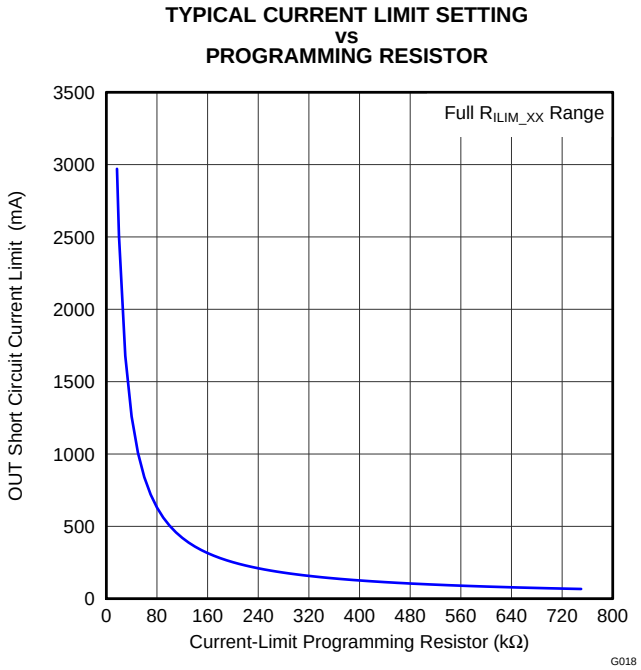


Figure 32.

Many applications require that the current limit meet specific tolerance limits. When designing to these tolerance limits, both the tolerance of the TPS2544 current limit and the tolerance of the external programming resistor must be taken into account. The following equations approximate the TPS2544 minimum / maximum current limits to within a few mA and are appropriate for design purposes. The equations do not constitute part of TI's published device specifications for purposes of TI's product warranty. These equations assume an ideal - no variation - external programming resistor. To take resistor tolerance into account, first determine the minimum / maximum resistor values based on its tolerance specifications and use these values in the equations. Because of the inverse relation between the current limit and the programming resistor, use the maximum resistor value in the I_{OS_min} equation and the minimum resistor value in the I_{OS_max} equation.

$$I_{OS\_min}(mA) = \frac{45{,}271}{(R_{ILIM\_XX}(k\Omega))^{0.98437}} - 30 \quad (2)$$

$$I_{OS\_max}(mA) = \frac{55{,}325}{(R_{ILIM\_XX}(k\Omega))^{1.0139}} + 30 \quad (3)$$

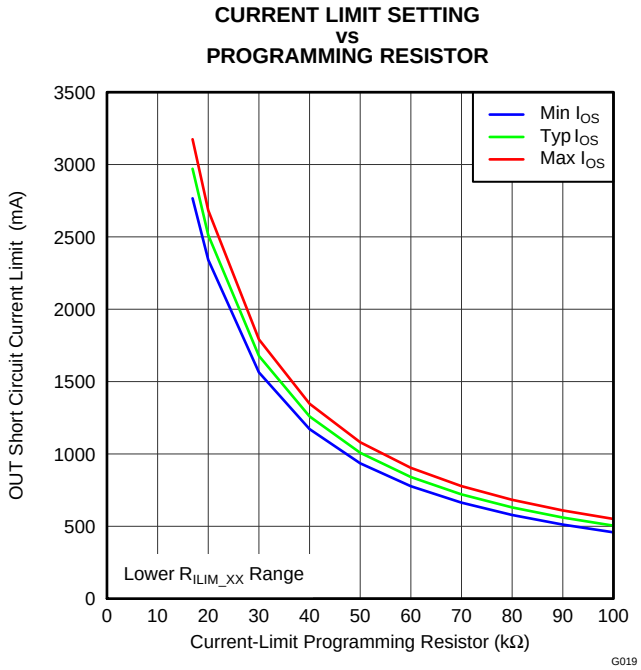


Figure 33.

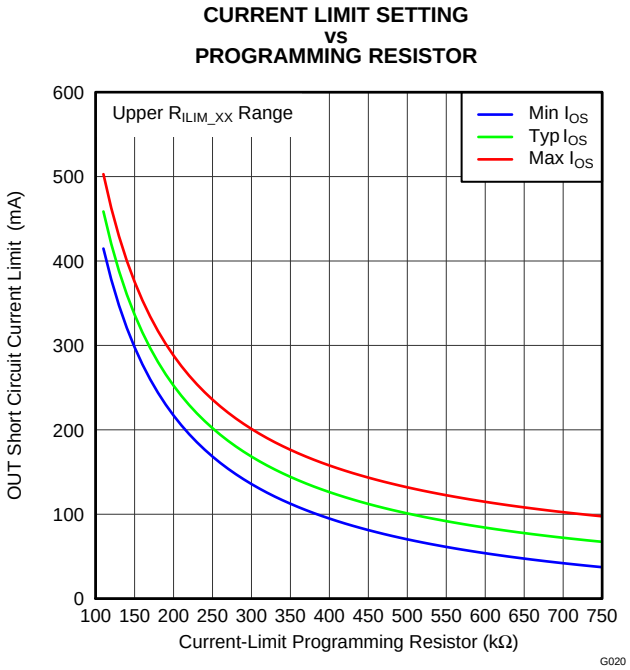


Figure 34.

The traces routing the R_{ILIM_XX} resistors should be a sufficiently low resistance as to not affect the current-limit accuracy. The ground connection for the R_{ILIM_XX} resistors is also very important. The resistors need to reference back to the TPS2544 GND pin. Follow normal board layout practices to ensure that current flow from other parts of the board does not impact the ground potential between the resistors and the TPS2544 GND pin.

FAULT Response

The $\overline{\text{FAULT}}$ open-drain output is asserted (active low) during an over-temperature or current limit condition. The output remains asserted until the fault condition is removed. The TPS2544 is designed to eliminate false $\overline{\text{FAULT}}$ reporting by using an internal deglitch circuit for current limit conditions without the need for external circuitry. This ensures that $\overline{\text{FAULT}}$ is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. Over-temperature conditions are not deglitched and assert the $\overline{\text{FAULT}}$ signal immediately.

Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted oscillations on the output due to input voltage drop from large current surges.

Thermal Sense

The TPS2544 protects itself with two independent thermal sensing circuits that monitor the operating temperature of the power distribution switch and disables operation if the temperature exceeds recommended operating conditions. The device operates in constant-current mode during an over-current condition, which increases the voltage drop across power switch. The power dissipation in the package is proportional to the voltage drop across the power switch, so the junction temperature rises during an over-current condition. The first thermal sensor turns off the power switch when the die temperature exceeds 135°C and the part is in current limit. The second thermal sensor turns off the power switch when the die temperature exceeds 155°C regardless of whether the power switch is in current limit. Hysteresis is built into both thermal sensors, and the switch turns on after the device has cooled by approximately 20°C. The switch continues to cycle off and on until the fault is removed. The open-drain false reporting output $\overline{\text{FAULT}}$ is asserted (active low) during an over-temperature shutdown condition.

REVISION HISTORY

Changes from Original (February 2013) to Revision A	Page
• Changed the device From: Preview To: Production	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS2544RTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2544	Samples
TPS2544RTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2544	Samples

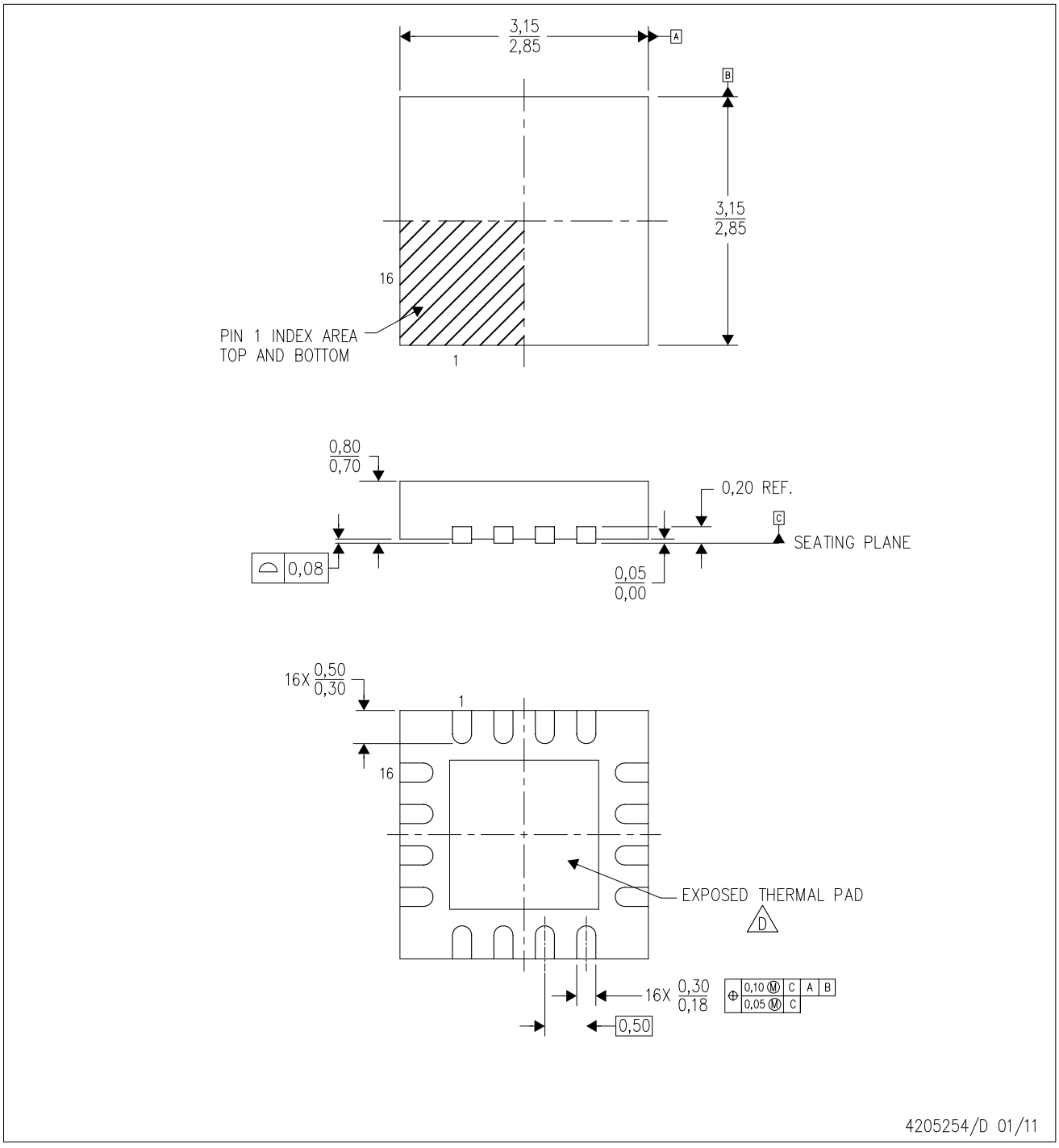
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

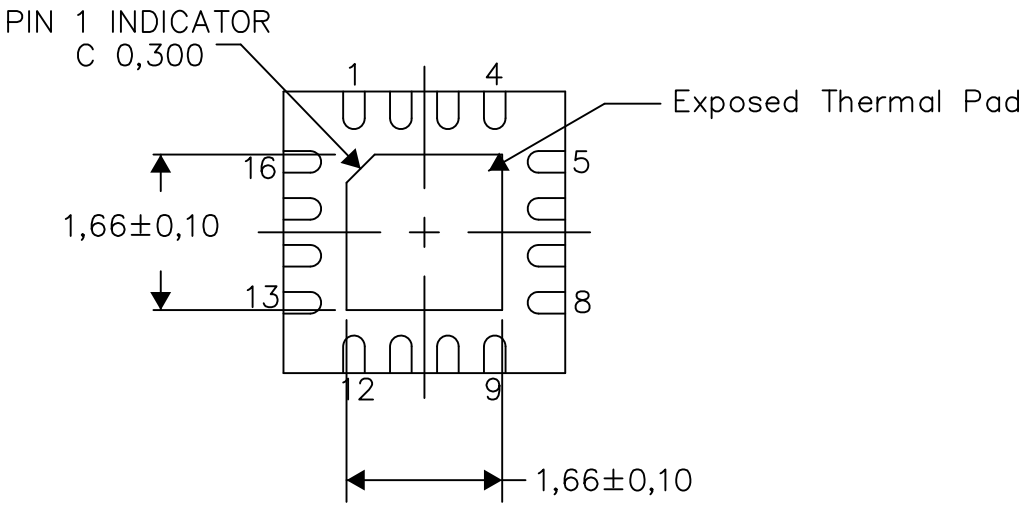
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



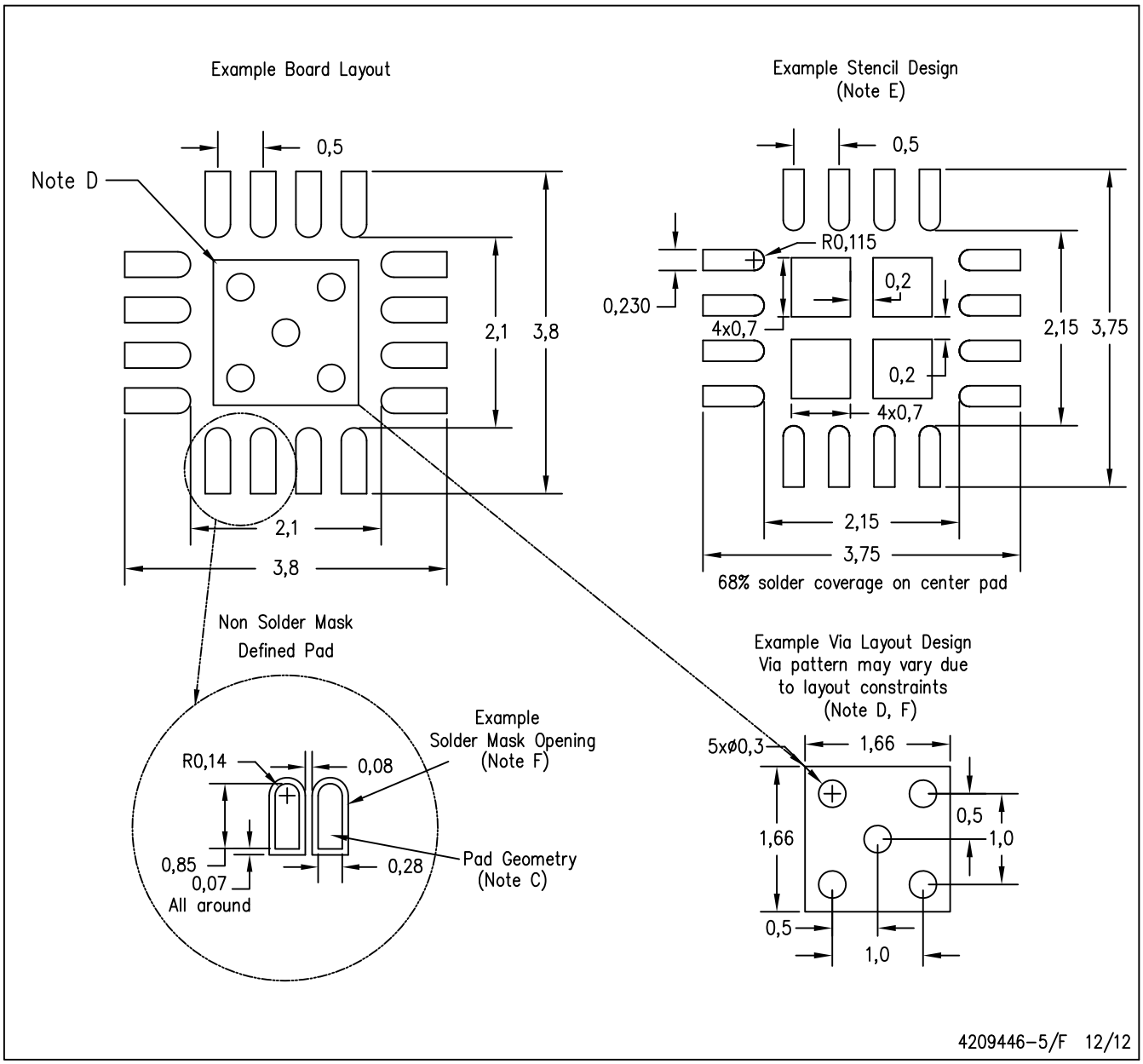
Bottom View

Exposed Thermal Pad Dimensions

4206446–5/K 12/12

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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